

DS50 Clock Fanout Module (CFM)

(Technical description)

1. Introduction

The DarkSide 50 (DS50) TPC Data Acquisition System includes one VME crate with ten (10) CAEN 8-channel 250 MS/sec v1720 modules along with several v1495 and v976 modules. The main purpose of the system is to digitize TPC detector signals within an acquisition gate of $\sim 300 \mu\text{s}$. All ADCs are running in parallel and require three (3) common control signals: Trigger, Run Enable and Clock. The expected ADC clock frequency is 50 MHz, but could be anything else. While Trigger and Run Enable could be either TTL or NIM level signals, the clock signals are differential LVDS level signals. The distribution of all signals has to be done with equal delays in a star-like topology. While distribution of TTL/NIM signals could be easily accomplished by using two CAEN v976 fanout modules, the LVDS fanout module is not available on the market. This document describes design of the 20-channel LVDS Clock Fanout Module (CFM) for the DS50 DAQ setup.

2. Clock Fanout Module main features

The CFM is implemented as a single width 6U VME module. There are two input connectors: LEMO 00 and 3-pin AMPMODU connector. The LEMO 00 connector accepts TTL/LVTTL/CMOS signals with selectable 50 ohm or 10Kohm termination. The AMPMODU connector accepts standard LVDS signal and is pin compatible with the CAEN v1720 ADC pinouts. The CFM features Texas Instruments CDCE906 PROGRAMMABLE 3-PLL CLOCK SYNTHESIZER / MULTIPLIER / DIVIDER which is a source of the output signals. The CDCE906 can be put in various modes including PLL Bypass and output divider. The CDCE906 receives its input frequency either from external source via LEMO 00/AMPMODU connector or from on-board 100 MHz OCXO AOCJY2 quartz crystal oscillator. The connector for the external clock source (LEMO/AMPMODU) is selected by two jumpers. The frequency source (external/internal) is selected by another jumper on the board. When running in the PLL mode, the CDCE906 can generate output frequencies in the range 190 kHz – 167 MHz. The CDCE906 has to be programmed via SMBus interface either before assembling of the PCB or on-board after assembly using Texas Instruments CDCE906/CDCE706 Programming Evaluation Module. For the initial setup with 50 MHz clock frequency the CDCE906 will be programmed to PLL Bypass mode with the output divider 1:2.

The CFM has two 34-pin 3M IDC connectors for the output LVDS signals. Each connector provides ten LVDS outputs. The pinout of the connectors allows splitting the flat ribbon cable in ten branches with 3-pin AMPMODU connector on each branch. There are two LEMO connectors for TTL/NIM clock outputs and one AMPMODU connector for additional LVDS clock output. The CFMs can be cascaded using either TTL or LVDS input/output connectors. There are four green LED indicators on the front panel showing signal source (EXT), selected input signal (TTL) and power supply voltages (+5V

and -12V). The CFM does not have any VME interface and only uses VME crate power supply. The block-diagram of the CFM design is shown in Figure 1. The PCB layout of the CFM is shown in Figure 2.

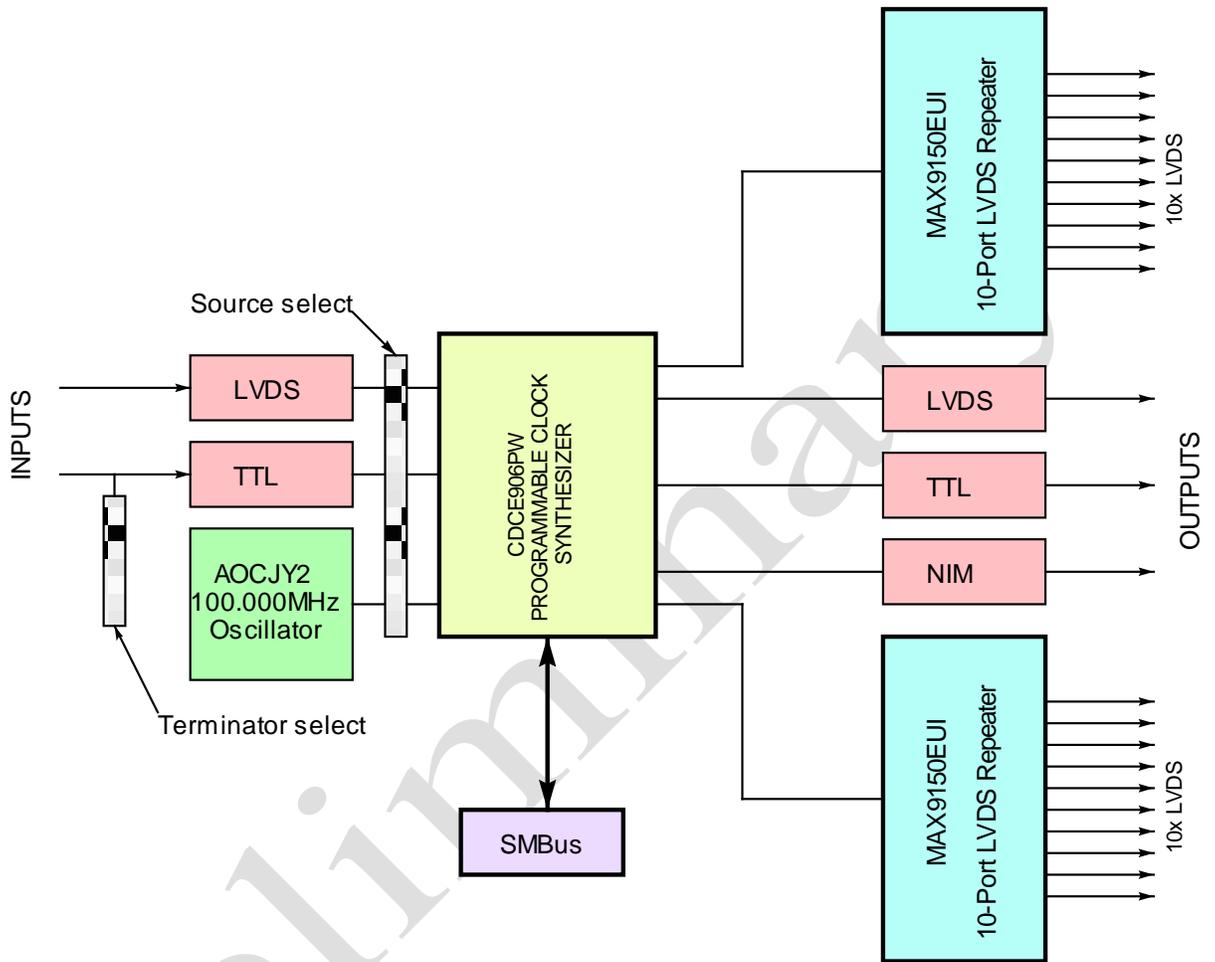


Figure 1. DS50 Clock Fanout Module

3. Specifications

The following are preliminary specifications for the Clock Fanout Module:

Inputs	TTL/LVDS
Termination	50 ohm/10K
Outputs	TTL/NIM/LVDS
Output delay (external mode)	20 ns
LVDS outputs skew	± 50 ps
LVDS output transition	1 ns
Number of LVDS outputs	20
Output frequency in PLL mode	190 kHz – 167 MHz
Frequency stability (short term)	± 5 ppb

Warm up time	3 min
Frequency stability (1 year)	± 100 ppb
Front panel LED indicators	"Ext.", "TTL", "+5V", "-12V"
Jumper selectors	"50 ohm/10K", "Ext./Int.", "TTL/LVDS"
Power consumption	+5V – 1.3A (warm up), 0.6A (continuous) -12V – 0.05A

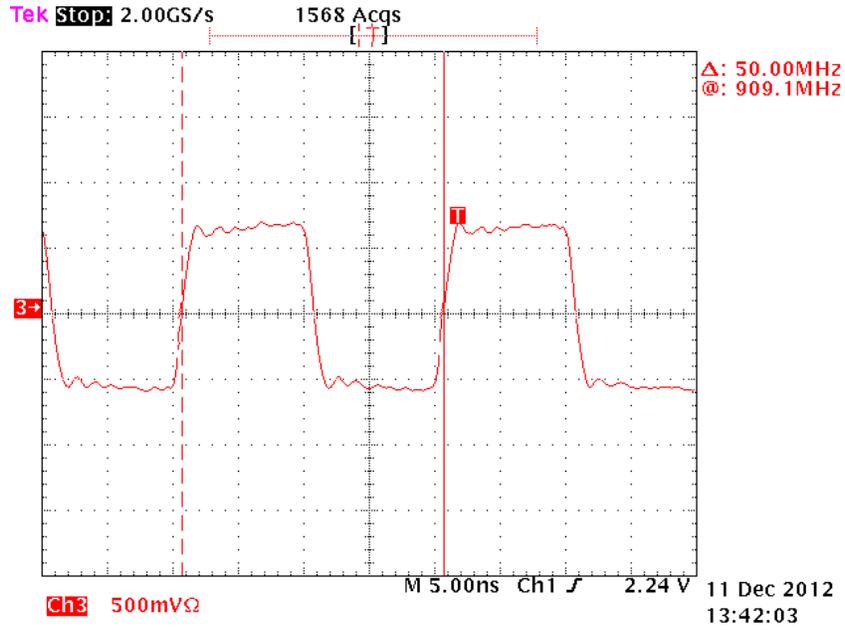


Figure 2. LVDS output signal (no load)

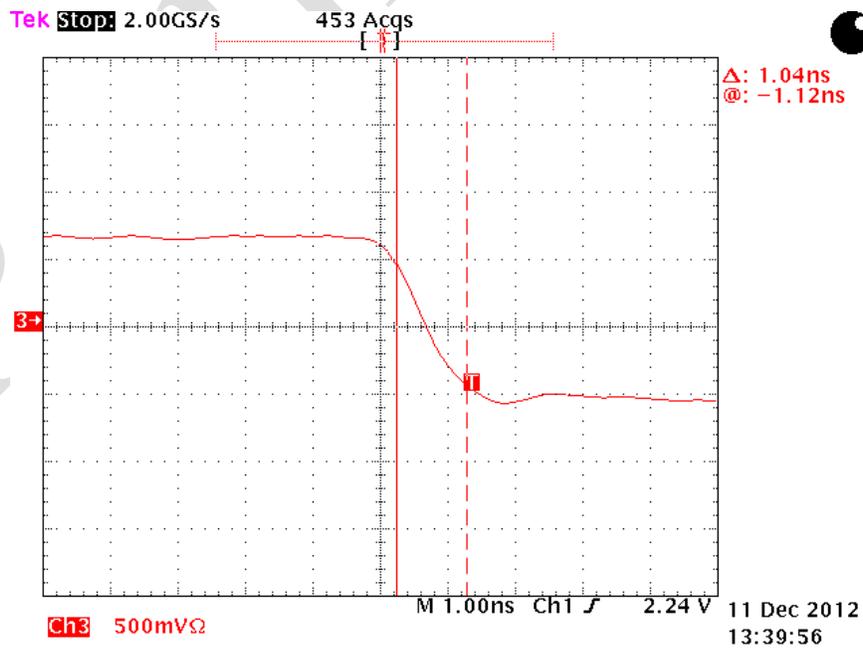


Figure 3. LVDS output signal transition time

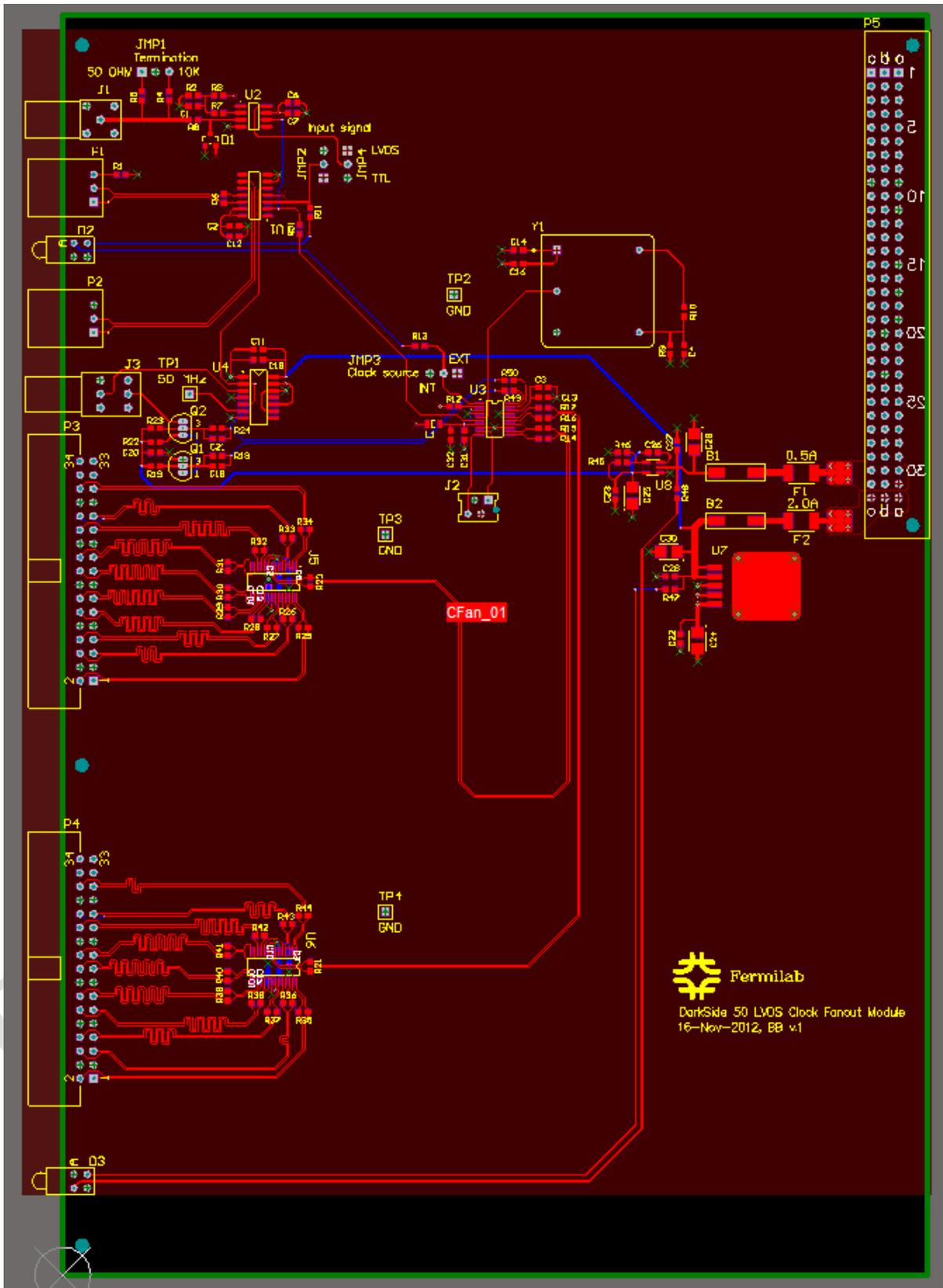


Figure 4. PCB layout of the CFM board

Table 1. AMPMODUII connector pinouts

Pin Number	Pin Name	Comment
1	IN+	LVDS signal
2	IN-	LVDS signal
3	GND	Reference ground

Table 2. 3M connector pinouts

Pin Number	Pin Name	Comment
1	Out0+	LVDS clock signal
2	Out0-	LVDS clock signal
3	GND	Reference ground
4	GND	Reference ground
5	Out1-	LVDS clock signal
6	Out1+	LVDS clock signal
7	Out2+	LVDS clock signal
8	Out2-	LVDS clock signal
9	GND	Reference ground
10	GND	Reference ground
11	Out3-	LVDS clock signal
12	Out3+	LVDS clock signal
13	Out4+	LVDS clock signal
14	Out4-	LVDS clock signal
15	GND	Reference ground
16	GND	Reference ground
17	Out5-	LVDS clock signal
18	Out5+	LVDS clock signal
19	Out6+	LVDS clock signal
20	Out6-	LVDS clock signal
21	GND	Reference ground
22	GND	Reference ground
23	Out7-	LVDS clock signal
24	Out7+	LVDS clock signal
25	Out8+	LVDS clock signal
26	Out8-	LVDS clock signal
27	GND	Reference ground
28	GND	Reference ground
29	Out9-	LVDS clock signal
30	Out9+	LVDS clock signal
31	NC	No connection
32	NC	No connection
33	NC	No connection
34	NC	No connection